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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/924,589	08/09/2001	Takahiro Kato	ASA-1018	3007

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EXAMINER	
BELLO, AGUSTIN	

ART UNIT	PAPER NUMBER
2633	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/924,589	KATO ET AL.	
	Examiner	Art Unit	
	Agustin Bello	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-7 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 09 August 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/9/01.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Baker (U.S. Patent No. 5,586,123).

Regarding claim 1, Baker teaches a receiving circuit unit (reference numeral 110 in Figure 1) for separating a multiplex electrical input signal from a first input port into electrical channel signals on a plurality of channels, delivering said separated electrical channel signals first output port (reference numeral 160 in Figure 1), and generating a clock signal (reference numeral 146 in Figure 1) from said multiplex electrical input signal; loopback path for taking out part of each of said separated electrical channel signals from said receiving circuit unit (reference numeral 106 in Figure 1); a selector (reference numerals 114, 116, 118 in Figure 1) for receiving each of said separated electrical channel signals via said loopback path and a plurality of input electrical channel signals fed from a second input port, and selecting said separated electrical channel signals from said second input port or said input electrical channel signals from said loopback path depending on a test mode signal fed from a switch port (e.g. under control of reference numeral 106 in Figure 1); and a transmitting circuit unit (reference numeral 112 in Figure 1) for multiplexing an output from said selector a time sharing manner to produce a multiplex electrical output signal, and delivering said output signal to a second output port (reference numeral 130 in Figure 1), said receiving circuit unit, said loopback path, said selector

and said transmitting circuit unit being formed on a single semiconductor chip (reference numeral 100 in Figure 1), whereby said semiconductor integrated circuit can be tested in a test mode (column 1 lines 6-11).

Regarding claim 2, Baker teaches another loopback path (reference numeral 106 in Figure 1) for taking out part of said clock signal generated from said receiving circuit unit; and another selector (reference numerals 114, 116, 118 in Figure 1) for receiving said generated clock signal via said other loopback path and a reference clock signal (reference numeral 132 in Figure 1) from a reference clock port, and selecting said generated clock signal from said other loopback path or said reference clock signal from said reference clock port depending on said test mode signal fed from said switch port (e.g. under control of reference numeral 106 in Figure 1), said other loopback path and said other selector being formed on said single semiconductor chip (reference numeral 100 in Figure 1).

Regarding claim 3, Baker teaches a clock generation circuit for generating an operation clock signal on the basis of said generated clock signal from said other selector (reference numeral 142 in Figure 1); a first-in first-out type buffer (reference numeral 108 in Figure 1) arranged to operate in synchronism with said operation clock signal from said clock generation circuit in order to absorb differences between timing change in said plurality of electrical input signals fed from said second input port; and a multiplexer (reference numeral 112 in Figure 1) for multiplexing said plurality of clocked electrical signals from said buffer in a time sharing manner.

Regarding claim 4, Baker teaches an output buffer (reference numeral 124 in Figure 1) connected between said first output port and said receiving circuit unit; and an input buffer (reference numeral 126 in Figure 1) connected between said second input port and said

transmitting circuit unit, said output buffer and said input buffer being formed on said semiconductor chip (reference numeral 100 in Figure 1), said two loopback paths being both connected between a junction of said output buffer and said receiving circuit unit and a junction of said input buffer and said transmitting circuit unit (as seen in Figure 1).

Claims 5-7 recite limitations similar to claims 1-4. Therefore, claims 5-7 are rejected for the same reasons as those stated in the rejection of claims 1-4.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Agustin Bello whose telephone number is (571) 272-3026. The examiner can normally be reached on M-F 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571)272-3022. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Agustin Bello
Examiner
Art Unit 2633

AB